Performance improvements with the new generation Intel Xeon E5-2600 v3 processor family and their impact on HPC workloads

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Keywords: Intel Xeon E5-2600 v3 processor, benchmarking, multicore, Haswell processor, AVX2

1. Introduction

The Intel Xeon E5-2600 v3 processor family is the first server Intel CPU supporting as DDR4 memory, AVX2 instruction set and transactional-memory model. The new extension to instruction set architecture AVX2 appears to be very useful for high-performance computing type of code. The new DDR4 memory subsystem brings additional benefits for memory intensive application increasing bandwidth of the whole platform.

The Intel Xeon processor E5-2600 v3 product family continues Tick-Tock successful development model by introducing the "Haswell" microarchitecture on proven 22nm process technology. Intel Xeon E5-2600v3 processor family is based on the same micro-architecture principles as its predecessor, however, becomes wider and armed in more resources. Intel Xeon E5-2600 v3 processor family has been designated for server market and utilized new server features optimized for performance improvement and reduction of energy consumption.

2. Architecture and System Configuration

For our study we have evaluated the 16-node cluster based on Intel Xeon E5-2697 v3. Each node is the dual socket server utilizing two Intel Xeon E5-2697 v3 processors. Essentially we have tested 14 cores 2.6GHz 145W CPU in FCLGA2011-3 package dedicated for server and workstations sockets. Intel PCSD Wildcat R2208WTTGSSPP platform has been selected as the platform of choice for the cluster. We populated each of the cluster nodes with 128GB of system memory (8x16GB DDR4-2133MHz). Every platform has deployed also enterprise Western Digital VelociRaptor 10k 500GB SATA hard disk drive.

The cluster system utilizes CentOS Linux 6.5 – Kernel 2.6.32-431.20.3.el6.x86_64. Latest versions of the Intel tools suite are installed. Intel Parallel Studio 2015 Initial Release and Warewulf HPC 3.5 packages provide all the necessary software components. The new compiler and libraries offer advanced vectorization support, including support for AVX2 and include Intel Parallel Building Blocks (PBB), OpenMP, High-Performance Parallel Optimizer (HPO), Interprocedural Optimization (IPO) and Profile-Guided Optimization (PGO). All performance tools and libraries provide optimized parallel functions and data processing procedures for high-performance applications.

3. CPU characteristic

The Intel Xeon E5-2600 v3 processor family has been manufactured on 22nm Hi-k metal Tri-Gate 3-D gate silicon technology. The Intel Xeon E5-2600 v3 family operates on the same frequency as the Ivy Bridge, but performance increases through core counts growth and via extension to instruction set architecture. The new support for the AVX2 has been added and it is a main driver of floating-point performance increase. To make this improvement powerful two fused multiply-add (FMA) units have been added. The FMA instruction can be issued in one cycle, against two cycles for separate multiply and add instructions. The FMA also improves accuracy, as the multiply operation performs infinite-precision results with no rounding in between. Comparing separate dependent multiply and add instructions latency versus FMA we go from eight to only five cycles. This is 60% instructions latency improvement versus preprocessor.

To support AVX2 extensions Haswell increases the bus width to 256 bits, this effectively doubles the L1 cache bandwidth for AVX type of entries but for integer this remains the same as in Sandy Bridge family.

Utilizing AVX2 and FMA, the Haswell processor does a peak of 16 double-precision flops per cycle, twice as big compared to Ivy Bridge and Sandy Bridge and four times bigger than Westmere and Nehalem. The AVX2 instruction set supports also integer operations with 256-bit vectors.

The Intel Xeon E5-2600 v3 is the first server processor to support DDR4 memory. Up until recently, supported by the previous generations of processors, DDR3 was the best performing type of memory, which served the IT industry for a number of years.

Transactional memory (TSX) improves the scaling efficiency of large coherent data structures and highly threaded workloads. Fundamentally transactional memory allows simultaneous access between execution threads without locking memory and serializing the access.

The Intel Xeon E5-2600 v3 processor has a number of other system enhancements such as integrated voltage regulator or AES-NI improvements, however unquestionably the most important enhancements for HPC field are FMA and DDR4 support.

4. Description of a problem solution

In this paper we compare five generations of Intel Xeon based cluster and critically evaluate the results we observed utilizing Intel Xeon E5-2600 v3 processor family based cluster versus predecessors. We compare previous generations of the cluster, study server platform features and Intel Instruction Set Architecture (ISA) and present a performance review. We also look into most effective utilization AVX2 and how the new memory subsystem exposes the situation when these new feature might be most effective way for performance increase. With that in mind, we then evaluate the results and discuss the implications for HPC type of code.

5. Results

We decided to use HPC Challenge benchmark (HPCC), NAS Parallel Benchmarks (NPB), Intel MPI Benchmark (IMB) to evaluate the five generations of clusters and therefore acquire the architectural perspective of cluster development in years: 2010-2015. Further to typical popular HPC synthetic benchmark, we decided to add to our testing scenario a subset of benchmarks recommended by PRACE consortium. As the majority of the benchmarks have been tailored to measure a system's floating-point computing performance using compute intensive routines as opposed to data intensive operations. We believe that best method to do objective validation of the system's capability is to run the benchmark applications. The subset of the benchmark from PRACE demonstrates how well the new system capability corresponds with real scientific applications. We have selected 5 applications' type benchmarks:

- AVBP
- VASP
- NAMD
- ELSA
- ORB75

The evolutionary improvement made on core count and memory subsystem reflects exactly the performance in real application type scenario. Nevertheless the most prominent enhancement of AVX2, which has also the biggest implication on HPC type of code, is Floating Point Multiply Accumulate. FMA substantially increases peak flops and provides perfected precision to further improve transcendental mathematics. They operate on scalars, 128-bit packed single and double precision data types, and 256-bit packed single and double-precision data types. It also increased accuracy compared to separated MUL and ADD. Double amount of FLOPs reached compared to previous generations are complemented by doubled cache bandwidth to feed FMA's execution units

Also DDR4 is bringing many benefits to the platform; but two highly expected benefits are an increase in memory bandwidth and power efficiency. Memory component makers standardize on new memory density technology every generation. With DDR4, most memory manufacturers will standardize on the 8Gb memory density. DDR3 will not have this level of density as standard which means that the largest memory density DIMMs in the future will only be available on DDR4 technology. The maximum memory speed supported by the Intel Xeon processor E5 2600 v3 is higher at all system capacities using 16 GB RDIMMs or 32 GB LRDIMMs. The benefit at 128GB is only one increment of memory speed performance, however at higher system capacities the memory speed advantage for Intel Xeon processor E5 2600 v3 is several increments of memory speed and can acheive up to 50% greater than systems supporting DDR3 with the previous generation of Intel Xeon processors.

6. Conclusions and future work

We conclusively see direct evidence of the doubling of the theoretical floating-point capacity with the new AVX2 capability to increase the HPC type of code e.g. very important BLAS function – DGEMM. For this subroutine, we observe the performance to near enough double over Intel SSE2 code. We also notice that new DDR4 memory subsystem provides significant improvement for bandwidth-oriented applications.

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