FPGA-BASED DVCPRO HD DECODER IMPLEMENTATION USING IMPULSE C

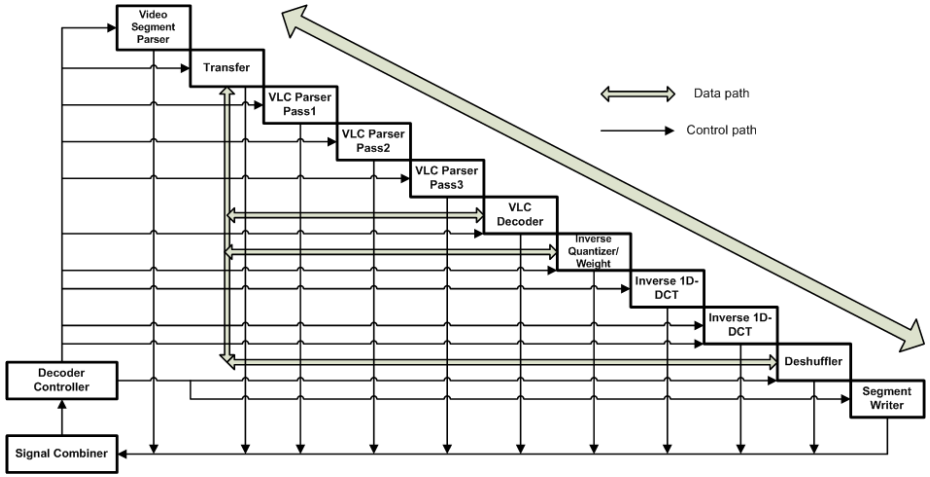
Sławomir Cichoń
Marek Gorgoń

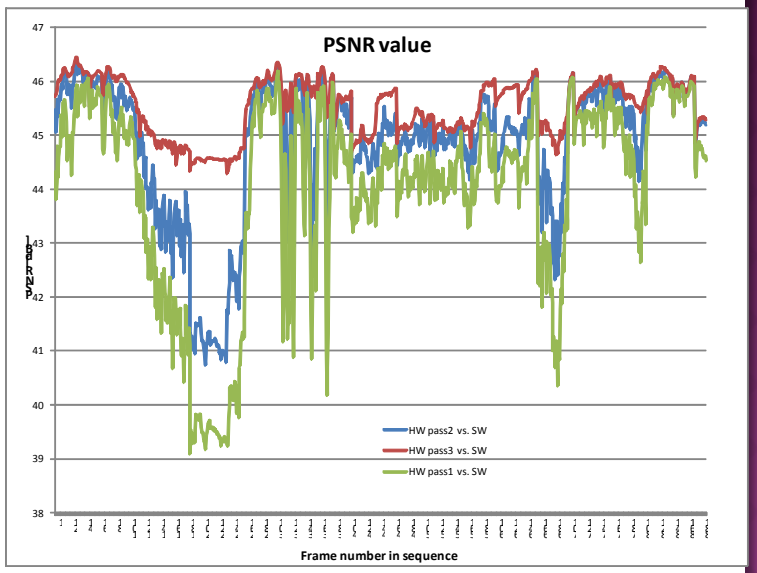
Department of Automatics, AGH UST Kraków

DVCPRO HD VIDEO CODING STANDARD

- The aim of this work was to implement in FPGA high resolution intra-frame video decoding algorithm
- Previously reported papers do not present solution for all three VLC passes
- In the current work high resolution (1440 x 1080) pixels and high bitrate (~100Mbps) compressed video bitstream is considered
- DVCPRO HD parameters:
  - Intra-frame coding only
  - 1920 x 1440 frame resolution
  - 25 fps (30 fps in US)
  - Discrete Cosine Transform-based
  - Lossy compression
  - Compression ratio ~ 5:1
  - Standardized in SMPTE 370M

DECODER IMPLEMENTATION





- Implemented using Impulse C High Level Language
- Tested on target board with Virtex-5 FPGA family (DRC AC2020)
- Fully compliant with SMPTE 370M
- All three VLC decoding stages (passes) implemented
- Running @ 200 MHz of FPGA clock frequency

FURTHER DETAILS DURING POSTER SESSION

THANK YOU ☺